REMARKS

These remarks are in response to the Office Action mailed on mailed on May 23, 2001, and for which a one-month extension is requested. The various points raised in the Office Action are discussed under the corresponding heading below. A Request for Declaration of Interference follows the discussions the rejection of claims 63-65. Additionally, a new claim has been added.

Objection to the Title and the Abstract

The title and Abstract of the present application have been amended along the lines of the suggestions made by the Office Action. In particular, the language added to the Abstract is based on that found on page 24, lines 3-8, of the present application.

Objection to the Drawings

The Office Action objected to the drawings under 37 CFR 1.83(a). It is believed that the drawing do show the claimed features. This is show below, under the "Support for the Proposed Count 1 in the Present Application" section of the Request for Declaration of Interference. In this section, reference is made to the elements of drawing that correspond to the features of the invention as specified in the claims.

Objection to the Disclosure

The Office Action noted several specific objections to the specification. In the "Cross-Reference to Related Applications" section inserted into page one by the Preliminary Amendment, the patent number of the immediate parent of the present application has been added. It is believed that the other updated status of applications cited in the present application have already been added by the Preliminary Amendment. The informality noted on page 11, line 31, has been corrected.

The "electronically" of the second line of claim 63 ahs been changed to --electrically--, thereby conforming with the remarks of the Office Action. The next section discusses the other amendments to this claim.

Rejections under 35 U.S.C. 112, second paragraph

The Office Action rejected claims 63-65 under 35 U.S.C. 112, second paragraph, raising several points. Concerning the "blocks, each having a plurality of sectors", in one embodiment this could correspond to the cylinders and sectors of the traditional disc system (see page 14, line 24 ff.) that the system of the present invention is preferably set up to emulate (see page 15, lines 7-12). However, to simplify the claim language, claims 63 and 65 have been amended to be written in terms of just the sector structure.

In one particular embodiment, the "address conversion table" and "means for converting ... and for accessing" respectively refer to the "sector defect map" and the controller. The invention specified in claim 63 is described under the "Defect Mapping" section that begins on page 14, line 12, of the present application, with sector substitution described between page 23, line 12, and page 24, line 8. For example, see page 24, lines 3-8:

> In yet another embodiment, the sector remapping is performed by the microprocessor. The microprocessor looks at the incoming address and compares it against the sector defect map. If a match occurs, it does not issue the command to the controller but instead substitute the alternative location as the new command.

Further support is provided below in the Request for Declaration of Interference.

Claim 63 has also been amended in order to clarify the relation between and connections of the various elements. The amending for this purpose has been kept rather minimal for purposes of the requested interference, but it is believed that that requirements of 35 U.S.C. 112, second paragraph, have been met.

Concerning the "means for" language of claim 63, the elements to which this refers for a particular embodiment is also given below under the "Support for the Proposed Count 1 in the Present Application" section of the Request for Declaration of Interference.

As described in the "Defect Mapping" section of the present application, the "logical sector address storage section..." may, for example, be part of the spare area 405 of Figure 4 or in the "DEFECT POINTER MEMORY FILE/HEADER COMPARE" section (509 in Figures 6 and 7) of the controller (31 in Figures 2, 6, and 7) depending on the embodiment.

Consequently, it is respectfully that the rejection of claims 63-65 under 35 U.S.C. 112, second paragraph, is not well founded and the claims are allowable.

New Claim

Claim 66 has been added. It is drawn to the same invention as claim 63, on which it is based, but is believed to more clearly present the various elements.

Reconsideration of the Office Action's rejection of claims 63-65, and consideration of new claim 66, is therefore respectfully requested, and an early indication of their allowability is earnestly solicited.

REQUEST FOR DECLARATION OF INTERFERENCE

It is respectfully requested that an interference be declared between the present application and U.S. patent no. 5,740,396 of Mason, referred to below as the "'396 patent". Claims 63-65 in their original form are exact copies of claims 1-3, respectively, of the '396. Claims 63 and 65 have been amend as described above for reasons related to 35 U.S.C. 112, second paragraph, and also to broaden them somewhat by removing the original "block" language. The new independent claim being added by this Amendment is patterned after some of the independent claims of the Mason patent but is not exactly the same. Claim 63 of the present application, which is based claim 1 of the '396 patent, is suggested as the count for the interference, as follows:

Count 1

A semiconductor disk device comprising:

a non-volatile, electrically programmable and erasable flash memory including a plurality of sectors, being a unit of erasure for the flash memory;

interface means for exchanging data and addresses with an external system;

an address conversion table for converting sector address information input from the external system into a physical sector number for identifying a sector of the plurality of sectors; and

means, connected to the address conversion table, for converting the sector address information input from the interface means from the external system into the physical sector number as identified by the address conversion table, and for accessing the flash memory according to the physical sector number.

35 U.S.C. 135(b)

Claim 63 of the present application was added by Preliminary Amendment, simultaneously with the filing of the present continued prosecution application on March 29, 1999. This is less than one year after the `396 patent was granted on April 14, 1998.

Effective Filing Date

As specified in the "Cross-Reference to Related Application" section added by the Preliminary Amendment filed on August 28, 1998, to the beginning of the application of which the present application is a continued prosecution application, the present application is entitled to an effective filing date of April 13, 1989 due to the benefit of:
U.S. Ser. No. 08/771,708, filed December 20, 1996, now patent no. 5,991,517,
U.S. Ser. No. 08/174,768, filed December 29, 1993, now patent no. 5,602,987,
U.S. Ser. No. 07/963,838, filed October 20, 1992, now patent no. 5,297,148,
U.S. Ser. No. 07/337,566, filed April 13, 1989.

The `396 patent is shown to have a United States filing date of February 8,1996, claiming priority from a Japanese patent applications with a date of February 16,1995. This over five years later than the April 13, 1989 effective filing date of the present application.

Therefore, it is requested that the interference be declared with the Applicants of the present application designated the senior party.

Claims Corresponding to the Proposed Count 1

The proposed count 1 is closely modeled on of claim 1 of the '396 patent. Claims 2 and 3 of the '396 patent are dependent on claim 1, reciting additional restrictions.

Support for the Proposed Count 1 in the Present Application

Count 1	Present Application
A semiconductor disk device comprising:	Block 29 of Figure 1A. The "disk" structure is described between p. 14, ln. 13, and p. 15, ln. 31.
a non-volatile, electrically programmable and erasable flash memory including a plurality of sectors, being a unit of erasure for the flash memory;	The described embodiments are all EEPROM memories. The sector (e.g. 211, 213, 215) as erase unit is shown in Figure 2 and described beginning on p. 8, ln. 7. p9, l4-5
interface means for exchanging data and addresses with an external system;	Host Interface 703 of Figure 8 or, in more detail, blocks 505, 507, 525/603 of Figures 6 and 7.
an address conversion table for converting sector address information input from the external system into a physical sector number for identifying a sector of the plurality of sectors; and	DEFECT POINTER MEMORY FILE 509 of Figures 6 and 7 in one embodiment. In another embodiment, spare portion 405 of Figure 5.

means, connected to the address conversion table, for converting the sector address information input from the interface means from the external system into the physical sector number as identified by the address conversion table, and for accessing the flash memory according to the physical sector number.

Generally, CONTROLLER 31 of Figures 1-2 and 6-8, with particular reference to elements 521, 517, 523/605 of Figures 6 and 7.

The invention specified in the claims is described in the present application mainly in the section entitled "Defect Mapping" that begins on page 14, line 12. The part of this section describes the structure of the traditional disk drive including the defect map table (p. 14, ln. 30) and how an embodiment of the present invention emulates the traditional disk structure (p. 15, ln. 7 ff.).

The operation of the controller in using the defect mapping is described with respect to Figures 6 and 7 between page 17, line 26, and page 23, line 11. This description is given mainly in terms of an embodiment for the mapping of single bits. The extension to sector mapping, as found in the proposed Count 1, is described between page 23, line 12, and page 24, line 8.

For these reasons, it is submitted to be clear that claim 1 of the `396 patent is supported by the present application disclosure, first filed on April 13, 1989.

`396 Patent Prosecution File History

A review of the file history of the `396 patent reveals that the material in neither the present application, the portion of the specification inserted by Preliminary Amendment, nor any of their descendants, was cited during the `396 patent application process.

Information Disclosure Statement

An Information Disclosure Statement is being prepared to include references cited in the parents to the present application and in the `396 patent. It is expected that this Statement, with forms 1449 and copies of references, will be filed with two weeks from the date hereof.

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Conclusion

A prompt declaration of the requested interference is respectfully requested. In the meantime, however, if the Examiner has any questions about this request, application or disclosure statements, a telephone call to the undersigned is invited.

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Respectfully submitted,

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APPENDIX

Marked up versions of amendments:

In the Specification

The material inserted by the Preliminary Amendment on page1, between lines 3 and 4:

Cross-Reference to Related Applications

This is a continuation of patent application serial no. 08/771,708, filed December 20, 1996, now patent no. [_,___;___] 5,991,517 which is a continuation of patent application serial no. 08/174,768, filed December 29, 1993, now patent no. 5,602,987, which in turn is a continuation of patent application serial no. 07/963,838, filed October 20, 1992, now patent no. 5,297,148, which in turn is a division of patent application serial no. 07/337,566, filed April 13, 1989, now abandoned.

The paragraph between on page 1, line 23, and page 24, line 5:

Optimized erase implementations have been disclosed in two copending U.S. patent applications. They are copending U.S. patent applications, Serial No. 204,175, filed June 8, 1988, by Dr. Eliyahou Harari, now patent no. 5,095,344, and one entitled "Multi-State EEprom Read and Write Circuits and Techniques," filed on the same day as the present application, Serial No. 07/337,579, filed April 13, 1989, now abandoned, by Sanjay Mehrotra and Dr. Eliyahou Harari. The disclosures of the two applications are hereby [incorporate] incorporated by reference. The Flash EEprom cells are erased by applying a pulse of erasing voltage followed by a read to verify if the cells are erased to the "erased" state. If not, further pulsing and verifying are repeated until the cells are verified to be erased. By erasing in this controlled manner, the cells are not subject to over-erasure which tends to age the EEprom device prematurely as well as make the cells harder to program.

In the Claims:

63.(Amended) A semiconductor disk device comprising:

a non-volatile, [electronically] electrically programmable and erasable flash memory including a plurality of [blocks, each block having a plurality of] sectors [and], being a unit of erasure for the flash memory;

interface means for exchanging data and addresses with an external system;

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an address conversion table for converting sector address information input from the external system into a physical [block] sector number for identifying a [block] sector of the plurality of [blocks] sectors; and

means, connected to the address conversion table, for converting the sector address information input from the interface means from the external system into the physical [block] sector number[,]as identified by [referring to] the address conversion table, and for accessing the flash memory according to the physical [block] sector number.

65.(Amended) The semiconductor disk device according to claim 64, wherein said address conversion table includes a logical sector address storage section and a physical [block] sector number storage section.

In the Abstract

ABSTRACT

A [system of Flash EEprom memory chips with controlling circuits] semiconductor disk device serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. In yet another embodiment, the sector remapping is performed by the microprocessor. The microprocessor looks at incoming address and compares it against the sector defect map. If a match occurs, it does not issue the command to the controller but instead substitutes the alternative sector. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

Pending Claims

63.(Amended) A semiconductor disk device comprising:

a non-volatile, electrically programmable and erasable flash memory including a plurality of sectors, being a unit of erasure for the flash memory;

interface means for exchanging data and addresses with an external system;

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an address conversion table for converting sector address information input from the external system into a physical sector number for identifying a sector of the plurality of sectors; and

means, connected to the address conversion table, for converting the sector address information input from the interface means from the external system into the physical sector number as identified by the address conversion table, and for accessing the flash memory according to the physical sector number.

64. The semiconductor disk device according to claim 63, wherein the sector address information includes a logical sector address.

65.(Amended) The semiconductor disk device according to claim 64, wherein said address conversion table includes a logical sector address storage section and a physical sector number storage section.

66. A semiconductor disk device comprising:

a non-volatile, electrically programmable and erasable flash memory including a plurality of sectors, wherein a sector is a unit of erasure for the flash memory;

an interface whereby data and addresses are exchanged with an external system;

a sector map comprising an identification between each of one or more of the sectors and a respective alternate sector;

a controller connected to the interface, the sector map and the memory, whereby in response to receiving an address from the interface for accessing one of said one or more sectors, the controller substitutes access to the respective alternate sector of the memory according to said identification.

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